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# New Low-Voltage CMOS Differential Difference Amplifier (DDA) and an Application Example

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***Abstract*—The paper presents a newly designed structure of a low-voltage differential difference amplifier (DDA). The novel implementation brings significant reduction of complexity in comparison to readily available operational amplifiers-based approach. It was designed in Cadence IC6 Spectre in 0.18 μm TSMC technology operating correctly with only ±0.9 V supply voltages and fabricated in EUROPRACTICE IC Service. Designed DDA features wide linearity and dynamics of output voltage together with operational bandwidth up to 100 MHz. Detailed simulation results and new voltage-mode second-order all-pass/notch filter are included to prove its superior behavior.**

***Keywords—analog electronics; all-pass/notch filter; differential difference amplifier; DDA; unity-gain follower***

## I. INTRODUCTION

Well-know circuit configurations with operational amplifiers (opamps) offer traditional linear signal operations such as summation and difference of voltage signals [1], [2]. However, structures provided using single opamp frequently require floating and grounded external resistors, while at the input of each branch an additional voltage follower is needed due to high-input impedance requirements. Many active building blocks (ABBs) with capability of processing sum and difference of input voltages have been presented in the literature. The ABB with multi-terminal linear voltage operations of sum and difference is called differential difference amplifier (DDA) [3], [4]. The conventional DDA operates as an amplifier and it processes two pairs of differential input voltages. Its CMOS topology was implemented by two differential NMOS pairs connected to single PMOS active load and high-gain output section (common source stage). However, some drawbacks of CMOS topology such as significant limitations in DC responses and asymmetry may occur, if low-voltage processes are used. Using full feedback [3], the DDA may work simply as differential-summing voltage follower. This ABB has wide range of applications in electronics working in voltage mode, such first-order all-pass filters [5], second-order universal biquad filters [6], or single-resistance-controlled-oscillators [7]. Recently, the DDA became a core circuit of various temperature sensor applications [8]-[10]. In addition, the DDA is also a key sub-block of other high-performance ABBs suitable for analog signal processing such as differential difference current conveyor (DDCC) [11], instrumentation amplifier [12], or voltage differencing differential difference amplifier (VDDDA) [13], [14], which recently received considerable attention in linear applications design, especially [15]-[17]. Moreover, the DDA is beneficially used as a sub-part of nonlinear active device so-called multiplied input differential difference amplifier (MIDDA) [18].

This contribution aims to introduce in comparison to opamp-based solution and topologies with commercially available devices such as AD830 [19] or AD8130 [20]: (i) a significantly simplified structure of DDA, (ii) its frequency features similar to commercially available devices (–3 dB cut-off frequency is up to 100 MHz) even under very low supply voltage, (iii) featuring high-impedance inputs and low-impedance output terminals, while (iv) the internal implementation does not require large amount of resistors. Usefulness of the designed DDA is demonstrated on novel voltage-mode (VM) filtering application.

## II. CIRCUIT DESCRIPTION

The schematic symbol of DDA with basic principle [3] of operation $v_o = A_0\,[(v_{p1} - v_{n1}) - (v_{p2} - v_{n2})]$ is shown in Fig. 1. In further text, DDA is discussed as differential-summing voltage follower providing operation $v_o = v_{p1} - v_{n1} + v_{n2}$, because negative feedback path is included in internal topology, which is beneficial for stability of the presented solution. In order to clarify the usage in further figures, it is shown as external connection, however, it cannot be disconnected. All input impedances of this device are supposed as infinite (in ideal case) and its output impedance should be close to zero. The DDA implementation using standard opamps leads to very complex (four opamps and five resistors) and also power

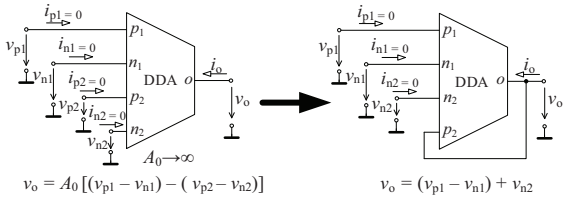


Fig. 1. Schematic symbol of differential difference amplifier (DDA) modified to differential-summing voltage follower [3].

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demanding solution. Some commercially available devices such as Analog Devices AD830 [19] or AD8130 [20] also provide required operation, but their internal topology is similarly complex (two OTAs and opamp in internal structure) and supply voltages are high (±5 V).

## III. Proposed Solution of DDA and its Analyses

The DDA shown in Fig. 2(a) was implemented in TSMC 0.18 µm CMOS technology with ±0.9 V power supply voltages and the parameters available in EUROPRACTICE IC Service design kit were used. The designed layout of the DDA with dimension 104.025 × 130.55 [µm] is shown in Fig. 2(b) . Note that all results were obtained with help of the Cadence IC6 Spectre analog design environment. Internal CMOS implementation of presented DDA is different from standard solutions [3]-[7]. The basic principle and novelty of operation results from folded cascode-based opamp design [21], where two additional NMOS and PMOS transistor pairs were added, while standard rail-to-rail opamp uses only single PMOS and NMOS differential pair. The reason for implementation of second group of PMOS and NMOS stages ($M_{p3\text{-}4}$, $M_{n3\text{-}4}$) comes from requirement for three (four) input terminals of the device. The operations of sum and difference of input voltages take place in form of output currents from differential pairs to folded cascode. The folded cascode stage is followed by amplifier ($M_7$) biased in class-A. The full structure performs unity gain when the internal on-chip feedback is closed. Then all three input signals are processed (sum and subtraction) and result is available at the low-impedance output terminal. Transistors $M_{p1} – M_{p4}$ and $M_{n1} – M_{n4}$ are medium threshold types (mvt), while the rest are of the standard type. Standard type of CMOS transistor in the respective technology has typical values of parameters (approximation when width » length): $V_{thP} = 0.48$ V, $K_{pP} = 39$ µA/V$^2$; $V_{thN} = 0.47$ V, $K_{pN} = 148$ µA/V$^2$. Typical values for medium threshold voltage types are: $V_{thP} = 0.2$ V, $K_{pP} = 53$ µA/V$^2$; $V_{thN} = 0.29$ V, $K_{pN} = 180$ µA/V$^2$. Designed values of aspect ratios (W/L) and other parameters in CMOS implementation suppose trade-off between power consumption (bias current $I_{bias} = 50$ µA), dynamics, linearity, and –3 dB frequencies up to 100 MHz. The quiescent total power dissipation of the proposed device is 1.72 mW. Next sections provide detailed Monte Carlo, temperature, and process variation results.

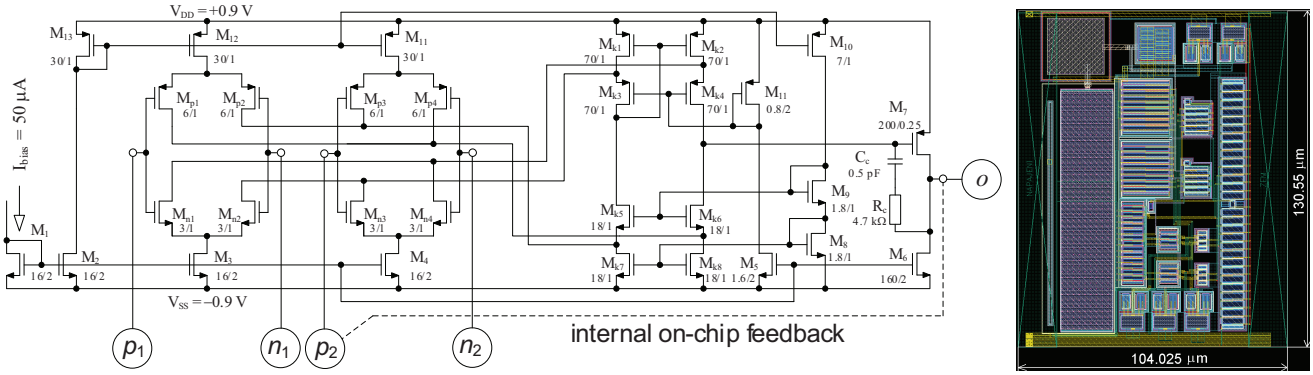
### A. DC Analysis

DC sweep of input voltages $v_{p1}$, $v_{n1}$, and $v_{n2}$ was tested in range ±600 mV under Monte Carlo mismatch analysis (100 runs), see Fig. 3. The DDA device (including feedback) was tested for the following discrete temperatures: 0, 25, 50 degrees and fast-fast, slow-slow, fast-slow, and slow-fast corner combinations, simultaneously, which in total generated 192 corners. For all three voltage transfers the limitations in dynamics are about ±300 mV and results yield maximal DC matching input offset approx. ±10 mV. Systematic DC offset does not overcome +0.24 mV (worst case from temperature and corner analyses). Note that corner and temperature effects are less significant than mismatch effects in this type of analyzed transfer responses (Fig. 3(b)).

### B. AC Analysis

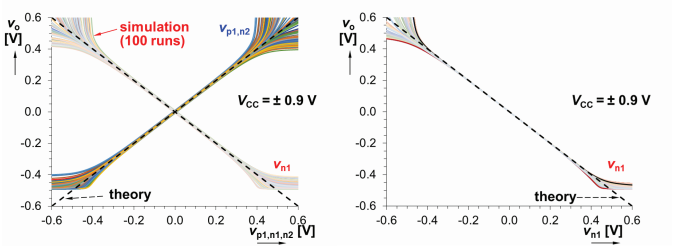
Results for temperature and corner analyses for transfers $v_{p1,n2} \rightarrow v_o$ and $v_{n1} \rightarrow v_o$, respectively, are shown in Fig. 4. Transfer features indicate cut-off (–3 dB) frequencies 93 and 96 MHz, both with dispersion ±24 MHz. This is an expected behavior, because RC network (its mismatch) was used for compensation in DDA structure (see $R_C$ and $C_C$ in Fig. 2). The compensation network of $R_C$ and $C_C$ connected in series is included to eliminate unwanted effects (peaking of magnitude) of load $R_L = 1$ kΩ with $C_L$ up to 15 pF ($C_L = 10$ pF noted in figures as estimation of effects from bond-pad, ESD protection, and experimental PCB prototype). On the other hand, mismatch has no significant impact on AC performance in comparison to corner and temperatures effects (see Fig. 5). This analysis yields very small deviations from nominal values of cut-off frequencies (approx. ±1.5 MHz). Effects of $C_L$ variation are given in Fig. 6.

Input and output impedances are also important parameters of the device. Input impedance is very high and not an issue (real part in order of GΩ). The output impedance $Z_o$ in dependency on frequency and mismatch or temperature/corner is shown in Fig. 7. It can be observed that the value of $Z_o$ is very low and does not overcome 5 Ω up to frequency 1 MHz.



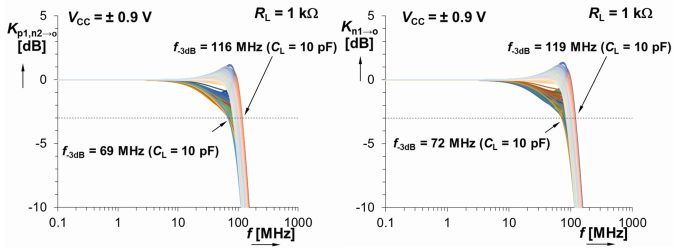

(a) (b)

Fig. 2. (a) CMOS implementation of DDA (with feedback - differential-summing voltage follower) based on 0.18 µm TSMC technology, (b) designed layout.



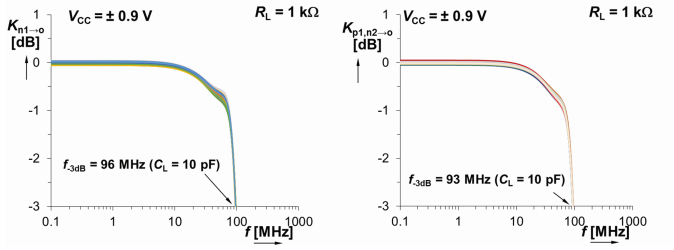

(a) (b)

Fig. 3. DC transfer responses: (a) Monte Carlo mismatch variation (100 runs) for $v_{p1,n1,n2} \rightarrow v_o$, (b) example for corner and temperature analysis for $v_{n1} \rightarrow v_o$.




(a) (b)

Fig. 4. AC transfer responses under corner and tempetature analysis: (a) transfer $v_{p1,n2} \rightarrow v_o$, (b) transfer $v_{n1} \rightarrow v_o$.




(a) (b)

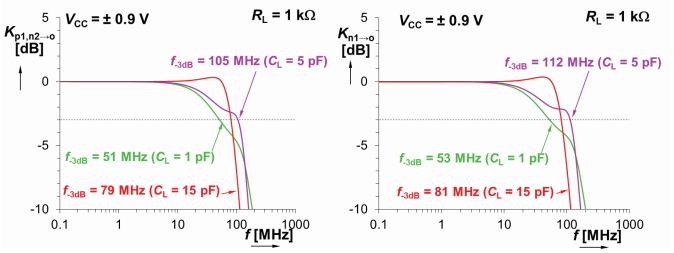
Fig. 5. AC responses under Monte Carlo mismatch test: (a) transfer $v_{p1,n2} \rightarrow v_o$, (b) transfer $v_{n1} \rightarrow v_o$.

In order to evaluate common mode rejection ratio (CMRR) of differential pair, input terminals $p_1$ and $n_1$ were excited by the same AC signal ($v_{p1} = v_{n1}$) from voltage source having zero DC component and connected to analog ground (0 V). Results of CMRR for mismatch analysis and for temperature and corner effects are shown in Figs. 8. CMRR (expressed as transfer response in figures) parameter is higher than 50 dB up to 10 MHz. Stability tests were provided for open loop gain bandwidth of the DDA. Phase margin was found to be from 53 to 76 degrees (all corners).

## IV. Proposed Application Example Using DDA

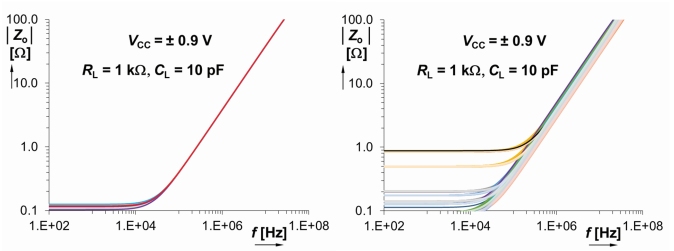
Figure 9 shows a novel VM second-order all-pass/notch filter. High-impedance input, low-impedance output, grounded capacitors, and simplicity are the most important benefits of the designed application example, which has the following transfer function:

$$K_{\text{all-pass/notch}}(s) = \frac{s^2 + s\dfrac{(3R_2C_2 - R_1C_1)}{R_1R_2C_1C_2} + \dfrac{1}{R_1R_2C_1C_2}}{s^2 + s\dfrac{2}{R_1C_1} + \dfrac{1}{R_1R_2C_1C_2}}, \quad (1)$$



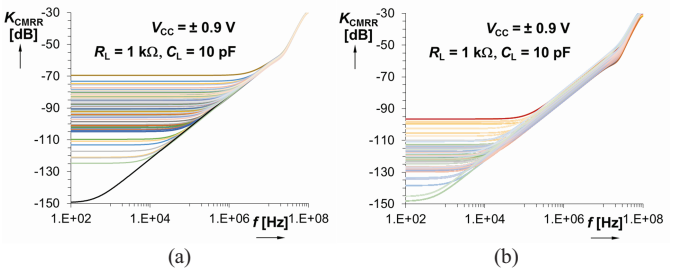

(a) (b)

Fig. 6. AC analysis of $C_L$ variation between 1 to 15 pF: (a) transfer $v_{p1,n2} \rightarrow v_o$, (b) transfer $v_{n1} \rightarrow v_o$.




(a) (b)

Fig. 7. AC analyses of output impedance: (a) Monte Carlo mismatch, (b) temperature and corner.




(a) (b)

Fig. 8. AC analyses of CMRR for $v_{p1} = v_{n1}$, $v_{n2} = 0$ V in reference to analog ground 0 V: (a) Monte Carlo mismatch, (b) temperature and corner effects.

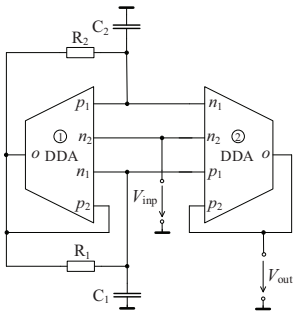
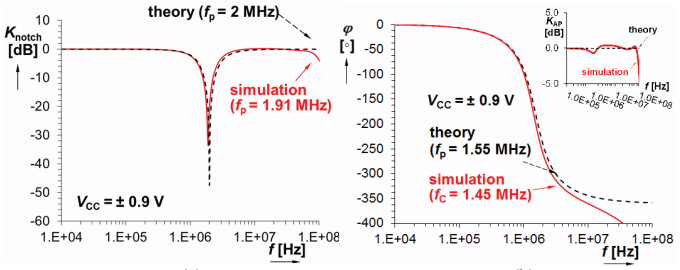



Fig. 9. Proposed all-pass/notch filter employing DDAs.

while the pole frequency and quality factor of the filter can be expressed as:

$$\omega_p = \sqrt{\frac{1}{R_1R_2C_1C_2}}, \quad Q_p = \frac{1}{2}\sqrt{\frac{R_1C_1}{R_2C_2}}. \quad (2a,b)$$

Routine analysis of (1) and (2) reveals that in order to obtain the notch filter operation, $Q_p = \sqrt{3}/2 \approx 0.87$ due to necessity of $R_1C_1 = 3R_2C_2$. Simple change of $C_1$ value causes possible reconfiguration of the transfer to the all-pass filtering




(a) (b)

Fig. 10. Resulting filter responses: (a) magnitude of notch filter, (b) magnitude and phase reponse of all-pass filter.

response, if $C_1 = 5 \cdot C_2$ and $R_1 = R_2$ are considered. Hence, (2a,b) change to $\omega_p = (5R_1R_2C_2^2)^{-1/2}$ and $Q_p = 0.5 \cdot \sqrt{(5R_1/R_2)}$, respectively. Note that several VM second-order all-pass/notch filter configurations are available in literature, however, for instance [22] and [23] require more complex active devices with many terminals and [24] requires larger number of ABBs than used in Fig. 9. As an example of particular results, Fig. 10(a) shows simulation results for notch filter (ideal $f_p = 2$ MHz, $C_1 = 15$ pF, $C_2 = 5$ pF, $R_1 = R_2 = 9.19$ kΩ). Frequency vs. magnitude and phase responses of all-pass filter (theoretical $f_p = 1.55$ MHz for $C_1 = 25$ pF, $C_2 = 5$ pF and $R_1 = R_2 = 9.19$ kΩ) are given in Fig. 10(b). From obtained results it can be seen that they are in very good agreement with the theory.

## V. Conclusion

In this paper, the DDA device uses different design principles than the conventional DDA available in [3], [11]. The challenges with significant asymmetry of limited DC response, especially for the positive polarity of input voltage occurred for very low supply voltages [13], are solved. Note that these issues are also solved in [4], however, the resulting topology seems to be several times more complex and requiring many bias sources than proposed in our paper. Proposed DDA offers wide linearity and dynamics approx. up to ±300 mV with maximal DC input offset ±10 mV, nominal frequency bandwidth > 90 MHz, very high input impedance, and output impedance < 5 Ω up to 1 MHz. Note that these features were obtained for low-voltage design in TSMC 0.18 µm CMOS process with supply voltage ±0.9 V. A new VM application example was introduced. Cadence IC6 Spectre simulation results confirm the feasibility of the proposed DDA and all-pass/notch filter.

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